

CMOS Implementation of 5T SRAM with Low Power Dissipation

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Abstract: SRAM is a very fast memory with low power consumption. The main objective of this work is to perform a 64-digit SRAM with 90 nm innovation. Execution depended on a granular perspective. SRAM's base module is similar to an N-MOS inverter, flip-flop, and semiconductor. We design this module according to the configuration rule of the λ format. Using Harvard technology, SRAM can easily retrieve information from memory. To create advanced rational circuits, it is important to see how an SRAM is assembled and how it works. The bottom line is that with 0.12 micron 90nm technology, we are developing a 5T SRAM and we can read and write. It is a fundamental part of a computer's central processing unit. RAM is a building block made up of several circuits. The 64-bit SRAM reader was developed with MICROWIND and DSCH2. With the MICROWIND program, the developer can design and simulate an integrated circuit at the physical description level. DSCH2 allows switching of digital logic design.

Keywords: SRAM, MICROWIND, N-MOS, C-MOS

I. INTRODUCTION

SRAM is an exceptionally quick memory with low force utilization. See how SRAM functions and how it is intended to make progressed rationale circuits. With this information and experience, we can plan more intricate incorporated circuits. We followed the rule of "equipment" in the plan of SRAM, which utilizes a secluded design comprised of more modest, more sensible squares, some of which can be reused. First we'll plan some SRAM as opposed to planning 64-bit SRAM, then, at that point we should collect some 64-bit SRAM to make 64-bit SRAM.

SRAM is the piece of a chip or microcontroller that plays out all the peruse and compose tasks of the circuit. SRAM is a basic piece of a PC's focal handling unit. Coordinated circuit is a circuit wherein every one of the substance of different circuits

are incorporated into a solitary chip. With the presentation of the incorporated circuit, every one of the peripherals and the chip were united in a solitary gadget called a microcontroller. All vital parts are collected in the microcontroller, with the goal that no other outer segments are required for its application, which saves reality for making gadgets. Microcontrollers likewise store information utilizing SRAM. The microcontroller has a base register, a SRAM, a memory, a control and a period unit. Because of the popularity for low force and low force convenient electronic gadgets, VLSI circuits have been recognized as a basic innovative need lately. Practically 90% of SRAM is comprised of exceptionally huge coordinated circuits.

II. LITERATURE REVIEW

John R Hu et al. [1] in this article, we present a deliberate way to deal with distinguish, foresee, and advance the plan cycle communication and to improve the general innovation to the chip/framework. This has delivered the best execution, execution and productivity for the GPU/SOC for elite registering, man-made reasoning (AI) and self-driving vehicle applications.

M. Horowitz et al. [2] Our test is clear: the quest for execution and the finish of voltage versatility have made execution, as opposed to number of semiconductors, the principle driver of additional upgrades in figuring power. To additional increment registering power, new specific preparing modules should be made and utilized productively.

M. Taylor et al. [3] Because of the disappointment of Dennard scaling, the level of a silicon chip that can switch at full recurrence diminishes dramatically with every age of cycles. This mass of utilization expects fashioners to ensure that consistently a huge segment of their chips are undoubtedly dim or feeble silicon; H. Either latent or fundamentally undervalued.

T. Chen et al. [4] AI exercises are pervasive in an assortment of fields and in an assortment of frameworks. Simultaneously, a little arrangement of AI calculations (particularly convolutional and profound neural organizations, like CNN and DNN) are ending up being at the cutting edge of many, numerous applications.

III. METHODOLOGY

A. Design approach of SRAM modules

Simply, to operate on k-bit SRAM, we can connect k 1-bit SRAMs. 64-bit SRAM is constructed using multiple 1-bit SRAMs as in our case.

Bottom-up approach

Small modules and there testing

Interconnection of different modules

1 Bottom-Up Approach

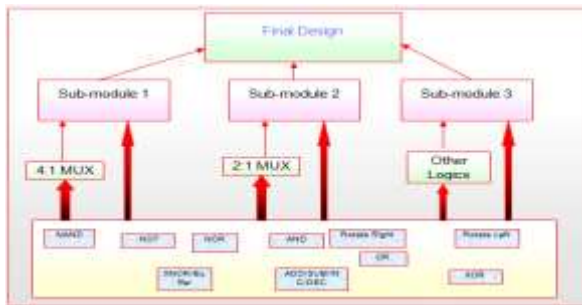


Fig. 1 Bottom-up approach designs

B. SRAM Design

64-bit SRAM is constructed using multiple 1-bit SRAMs. Simply, to operate on k-bit SRAM, we can connect k 1-bit SRAMs.

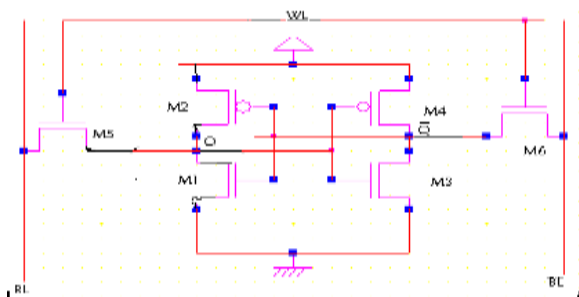


Fig. 2 Block diagram of a 1-bit SRAM.

C. Read Operation

In 6T SRAM, the stored value and its inverse are used in the evaluation to determine the stored value so that the cell has a differential read operation. Before processing a read operation, the word line is kept low (to ground) and the two bit lines

connected to the cell via transistors M5 and M6 are preloaded up (to VCC).

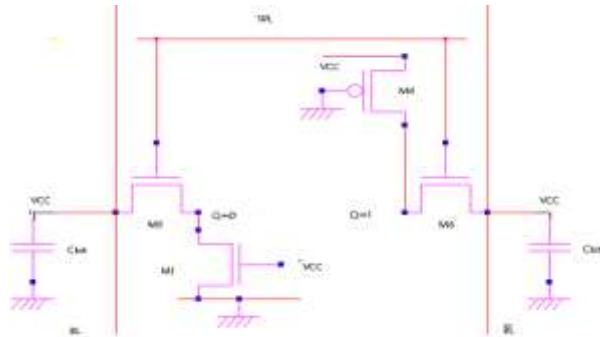


Fig. 3 Six-transistor SRAM cell of read operation

In Fig. 3, the Cbit is a capacitor representing the capacitances on the bit lines, which are several orders of magnitude greater than the capacitance of the cell. The cell capacity was represented here only by the value held by each inverter ($Q = 0$ or $Q = 1$). The next step of the reading operation consists in pulling the word line upwards while activating the bit lines. This turns on the access transistors (M5 and M6) and connects the memory nodes to the bit lines. We see that the right storage node (the reverse node) has the same potential as $(BL)^-$ and therefore no charge transfer takes place on this side.

D. Write Operation

For a standard 6T SRAM cell, writing is done by lowering one of the bit lines to ground and the other is loaded up while asserting the word line. To write a '0' BL is lowered, while writing a '1' requires $(BL)^-$ to be lowered.

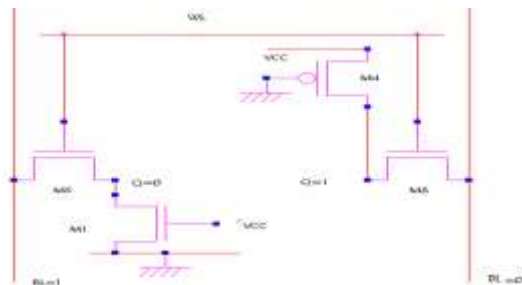


Fig. 4 Six-transistor SRAM cell at the onset of write operation

E. 5T SRAM

Fig. 5 shows the plan of a 5T SRAM cell where the qualities 1 or 0 ought to be set on the bit line if the secret key choice line changes to 1. The square of the two inverters takes on the bit line esteem. In the following condition of the SRAM, the select word line gets back to 0, the SRAM is in the compose state, and the select sign word line ought to be enacted, however no data ought

to be forced on the bit line. For this situation, the worth of the put away information is sent to the bit line.

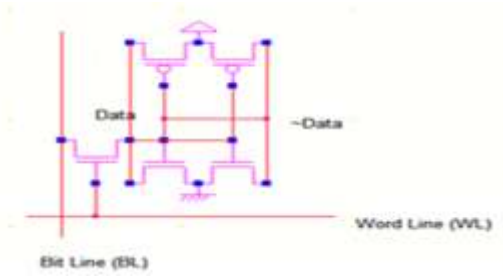


Fig. 5 schematic of Design of 5T SRAM Cell

F. 64-BIT SRAM

This segment gives a definite investigation of the 64-bit SRAM cell reenactment. We gauge the impact of the SRAM cartridge on power scattering. The SRAM cell plot is planned and carried out utilizing Micro Wind 3.1. The plan was recreated with .12µm and 90nm CMOS innovation. Then, we plan a 64-bit memory utilizing a 5T SRAM cell and the outcome is contrasted with an ordinary 6T SRAM cell.

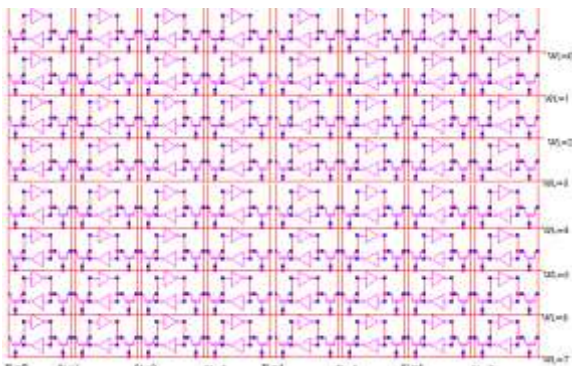


Fig. 6 64 BIT 6 T SRAM

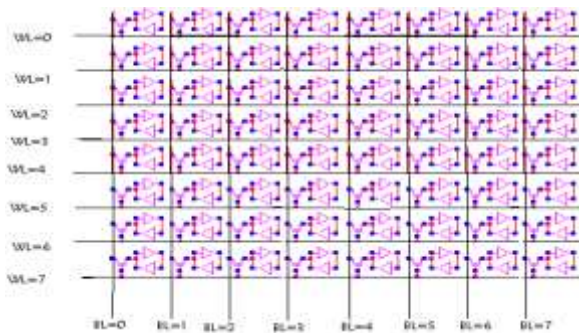


Fig. 7 Block diagram of 5T 64-bit SRAM.

1 Design Rules Classification

Design rules are a bunch of mathematical determinations that direct the plan of the format veils. A plan rule set gives mathematical SRAM.

Minimum width

Minimum spacing

Surround

Extension

All widths, spacing, and distances are written in the form of $m \lambda$.

G. CMOS Layout Design Rules

Any structure format configuration should stick to a bunch of format configuration decides that decide the mathematical imperatives forced on the structure levels by innovation and assembling measures. The setup architect should keep these standards to guarantee a particular return for the completed item, which is H. A specific level of satisfactory chips from a creation clump. A plan that disregards a portion of the format configuration rules can in any case bring about a useful chip, yet execution ought to be more slow because of irregular varieties all the while.

1 CMOS Process Layers

| Layer | Color | Representation |
|----------------------|---------|----------------|
| Well (p,n) | Yellow | |
| Active Area (n+,p+) | Green | |
| Select (p+,n+) | Green | |
| Polysilicon | Red | |
| Metal1 | Blue | |
| Metal2 | Magenta | |
| Contact To Poly | Black | |
| Contact To Diffusion | Black | |
| Via | Black | |

Fig. 8 CMOS process Layer

H. CMOS Inverter

Here, the system for planning the design of a CMOS inverter cover is characterized bit by bit. The circuit comprises of a nMOS and a pMOS semiconductor; According to the plan rules, we need to make the individual semiconductors. Assume we attempt to fabricate the inverter with least size semiconductors. The base size of the dispersion contact (needed for source and channel associations) and the base distance between the dissemination contact and the two edges of the dynamic region decide the width of the dynamic region. The width of the polysilicon line across the dynamic region (which is the entryway of the semiconductor) is by and large viewed as the base shaft width. Along these lines, the absolute length of the dynamic not set in stone basically by the accompanying total: (least post width) + 2 x (least separation from the shaft contact) + 2 x (least separation from the contact to the edge of the dynamic surface). The base size of n wells is given by the dynamic pMOS region and the pMOS semiconductor should be set in a space of n wells and the base cross-over of n wells is n

+. The distance between the nMOS semiconductor and the pMOS is controlled by the base distance between the dynamic region n + and the well n. The polysilicon doors of the nMOS and pMOS semiconductors are for the most part adjusted. In the design of the cover, the last advance is the neighborhood metal associations for the yield hub and for the VDD and GND contacts. Note that the n-well zone should likewise have a VDD contact to be appropriately enraptured.

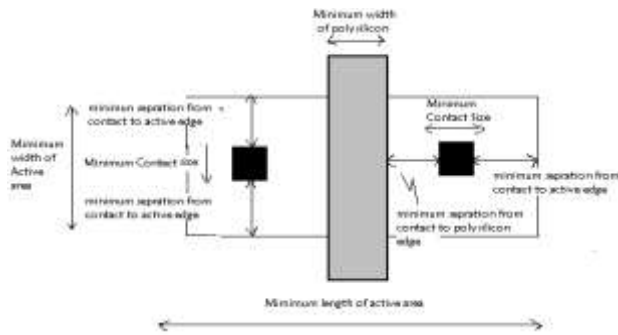


Fig. 9 Design rule constraints which determine the dimensions of a minimum size transistor.

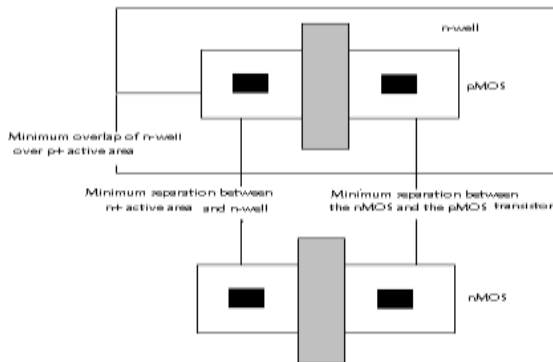


Fig. 10 Placement of one nMOS and one pMOS transistor.

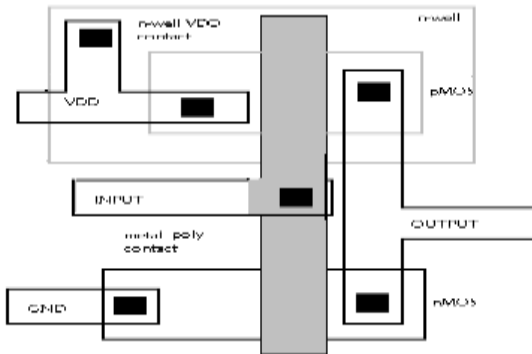


Fig. 11 Complete mask layout of the CMOS inverter

The main topics discussed are:

Power-consumption components

Static power consumption

Dynamic power consumption

Power-Consumption Components

In PC frameworks, high frequencies rigorously limit energy utilization. Hence, the force utilization of every gadget on the board ought to be kept to a base. Force computations decide cooling/heat sink necessities, current prerequisites, power supply size, and gadget choice rules. The most extreme solid working recurrence cannot really set in stone from the force estimations. In a CMOS circuit, the force utilization is dictated by two parts:

- Static power consumption
- Dynamic power consumption

1 Static Power Consumption

In general, a CMOS inverter is used for all low voltage devices in the input and output stages. For a clear understanding of static power consumption, please refer to the CMOS inverter modes shown in the figure 12.

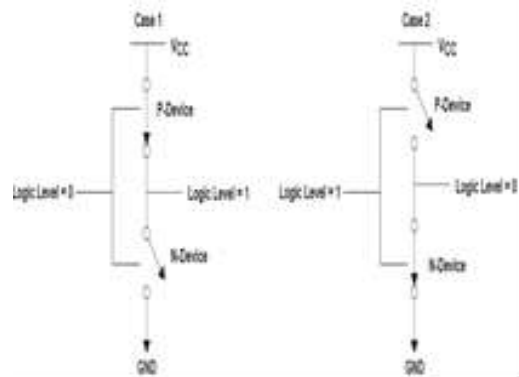


Fig. 12 CMOS Inverter Mode for Static Power Consumption

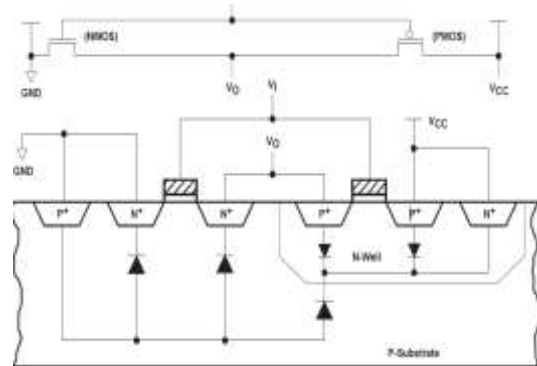


Fig. 13 Model Describing Parasitic Diodes Present in CMOS Inverter

Figure 13 shows the parasitic diodes between the well N and the substrate. The parasitic diodes are framed by the source-channel dispersion and the N-well dissemination. Since parasitic diodes are converse one-sided, just their spillage flows add to the

utilization of friction based electricity. The spillage current (I_{lkg}) of the diode is depicted by the accompanying condition,

$$I_{lkg} = i_s(e^{qV/kT} - 1) \tag{4.2}$$

Where:

i_s = reverse saturation current

V = diode voltage

k = Boltzmann’s constant (1.38 × 10⁻²³ J/K)

q = electronic charge (1.602 × 10⁻¹⁹ C)

T = temperature

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation 4.3.

$$P_S = \sum (\text{leakage current}) \times (\text{supply voltage}) \tag{4.3}$$

Most CMOS datasheets give a greatest ICC in the scope of 10 mA to 40 mA, which incorporates all spillage flows and other circuit attributes that might require static current not considered in model d. Basic inverter. The ICC spillage current (gadget current) related with the stockpile voltage brings about static force utilization in CMOS gadgets. This static force utilization is characterized as a tranquil state or PS and can be determined from the condition 4.4.

$$P_S = V_{cc} \times I_{cc} \tag{4.4}$$

Where:

V_{CC} = supply voltage

I_{CC} = current into a device (sum of leakage currents as in equation 4.2) another source of static current is DICCC. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

Dynamic Power Consumption

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (PT), and capacitive-load power consumption (PL).

1. Transient Power Consumption

Consequently, the unique inventory current is dictated by the charge and release current of the charge limit and the inner limit of the coordinated circuit, and the transient force utilization can be determined utilizing a condition 4.5.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{SW} \tag{4.5}$$

Where:

P_T = transient power consumption

V_{cc} = supply voltage

f_I = input signal frequency

N_{sw} = number of bits switching

C_{pd} = dynamic power-dissipation capacitance

In the case of single-bit switching, N_{sw} in equation 4.5 is 1.

2. Capacitive-Load Power Consumption

When charging the external load capacity, additional energy is consumed, which depends on the switching frequency. If all the outputs have the same load and switch at the same output frequency, the following equation can be used to calculate this power:

$$P_T = C_L \times V_{CC}^2 \times f_o \times N_{sw} \tag{4.6}$$

(C_L is the load per output)

Where:

P_L = capacitive-load power consumption

V_{CC} = supply voltage

f_O = output signal frequency

C_L = external (load) capacitance

N_{sw} = total number of outputs switching

Equation 4.7 is used to calculate capacitive-load, in the case of different loads and different output frequencies at all outputs. Then Power consumption:

$$P_L = \sum (C_{Ln} \times f_{on}) \times V_{cc}^2 \tag{4.7}$$

Where:

S = sum of n different frequencies and loads at n different outputs

f_{on} = all different output frequencies at each output, numbered 1 through n (Hz)

V_{cc}= supply voltage (V)

C_{Ln} = all different load capacitances at each output, numbered 1 through n.

In this way, dynamic force utilization (PD) is the amount of these two force utilizations and can be communicated as displayed in equation4.8, condition 4.9 (single-bit exchanging), and condition 4.10 (different bit exchanging with variable burden and variable yield frequencies),

$$P_D = P_T + P_L \tag{4.8}$$

$$P_D = (C_{pd} \times V_{CC}^2 \times f_I) + (C_L \times V_{CC}^2 \times f_o) \tag{4.9}$$

$$P_D = [(C_{pd} \times f_I \times N_{SW}) + \sum (C_{Ln} \times f_{on})] \times V_{cc}^2 \tag{4.10}$$

Where:

C_{pd} = power-consumption capacitance (F)

F_i = input frequency (Hz)

F_{on} = all different output frequencies at each output, numbered 1 through n (Hz)

N_{sw} = total number of outputs switching

V_{cc} = supply voltage (V)

C_{Ln} = all different load capacitances at each output, numbered 1 through n.

Total power consumption is the sum of static and dynamic power consumption.

$$P_{tot} = P_{(static)} + P_{(dynamic)} \quad (4.11)$$

There are a few different ways to limit energy utilization. In contrast to Bipolar and BiCMOS, we can just utilize CMOS, which can decrease DC power utilization until scattering. The utilization of gadgets of least size is a benefit for misfortunes since it is corresponding to the dispersion region. One of the framework plan contemplations is the decision of low force gadgets, with frameworks today utilizing gadgets in the 1.5V to 3.3V DC range. Dynamic force utilization can be restricted by decreasing the recurrence with which the rationale is synchronized, the stock voltage and the exchanging limit.

Exchanging Capacity - When signs change rationale state in a CMOS semiconductor, energy is drawn from the force supply to charge the heap limit from 0 to Vdd. For the inverter, the force drawn from the inventory is scattered as warmth in the pMOS semiconductor during the charging interaction. Energy is required when the heap is moved against a potential. Henceforth $dE = d(VQ)$. At the point when the inverter yield changes from rationale 0 to 1, the heap limit is charged. The energy taken from the force supply during the charging cycle is given by,

$$dEp = d(VQ) = Vdd.dQL$$

Since the power supply provides power at a constant voltage Vdd. Now, since $QL = CL.VL$, we have:

$$dQL = CL.dVL \text{ and } dEP = Vdd.CLdVL$$

Integrating for full charging of the load capacitance,

$$Ep = \int_0^{Vdd} Vdd.CL.dVL$$

Thus a total of $C_L.Vdd$ energy is drawn from the power source. The energy EL stored in the capacitor at the end of transition can be computed as follows:

$$dEL = d(VQ) = VL.dQL$$

where V_L is the instantaneous voltage across the load capacitance, and Q_L is the instantaneous charge of the load capacitance during the loading process. Therefore,

$$dEL = VL.CLdVL$$

Integrating for full charging of the load capacitance,

$$EL = \int_0^{Vdd} CL.VL.dVL \\ = (CL.V^2dd)/2$$

only half of the energy drawn from the power supply is stored in the load capacitance; the rest is dissipated as heat.

IV. RESULTS

A. Functional Simulation

MICROWIND supports entire front-end to back-end design flow.

For the front-end plan, we have DSCH (Digital Schematic Editor), which has a coordinated example based test system for computerized circuits. The client can likewise make simple circuits and convert them to SPICE records and utilize outsider test systems like WinSpice or pSPICE. DSCH can change over computerized circuits into Verilog records, which would then be able to be integrated for FPGA/CPLD gadgets from all makers. The Verilog document itself can be aggregated for format change to MICROWIND.

The 64-bit 5T execution utilizing 90nm innovation enjoys the benefit of lessening power dispersal and decreasing deferral and region. In an examination between 64-bit SRAM 6T and 64-bit SRAM 5T, we show that 64-bit SRAM 5T diminishes power misfortune in 90nm innovation.

B. Layout design of nmos Transistor

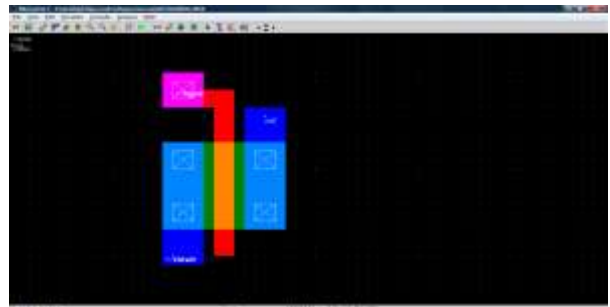
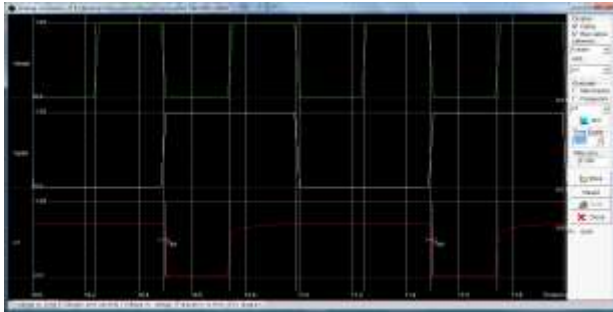


Fig. 14 Layout design of Nmos transistor

Here Vdrain is the drain voltage, Vgate is the gate voltage and out is the output of Nmos

1. Simulation of nmos Transistor



Voltage Vs time wave form of nmos transistor

Fig. 15 shows simulation of Nmos transistor. This is a voltage vs time waveform of nmos transistor. Here a clock gives in Vgate and also in Vdrain. Output taken from out port. When Vgate is high Vdrain is pass through Nmos and reach in out. When Vgate is low no any transition take place.

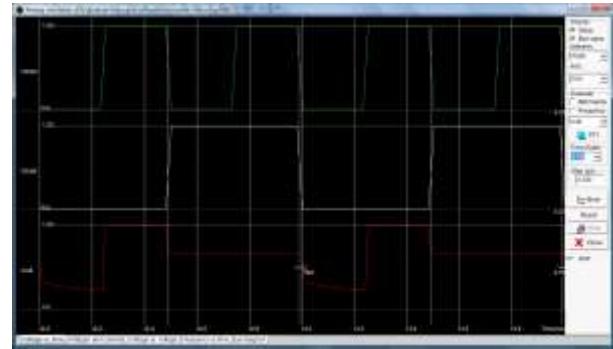
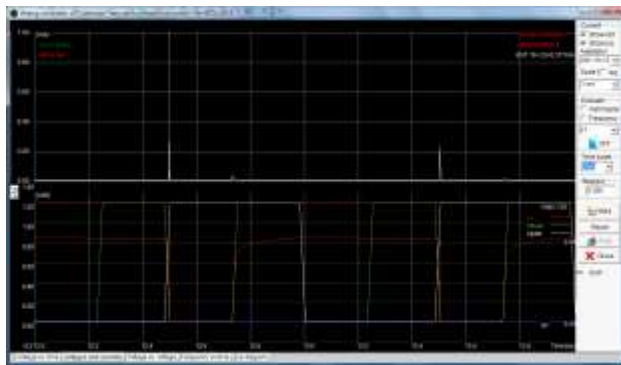


Fig. 18 Voltage Vs Time pmos transistor

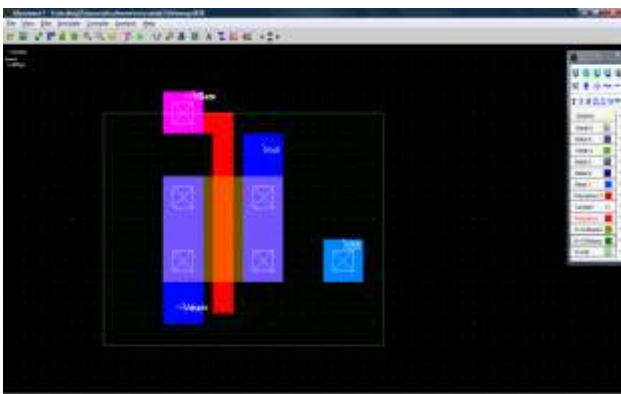
When Vgate is low, Vdrain is show on Vout. When Vgate is high no any transition.



16 Voltage Vs Current nmos transistor

Fig 16 shows simulation of nmos transistor. This is a voltage vs current waveform of nmos transistor.

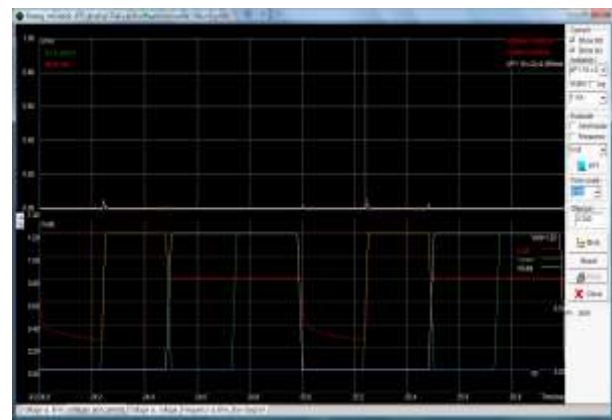
C. Layout of pmos transistor



Layout of pmos transistor

Here Vdrain is the drain voltage, Vgate is the gate voltage and Vout is the output of Pmos.

1. Simulation of pmos Transistor



19 Voltage Vs Current wave form of pmos transistor

Vgate is high , Vout is also high .

D. Layout design of inverter

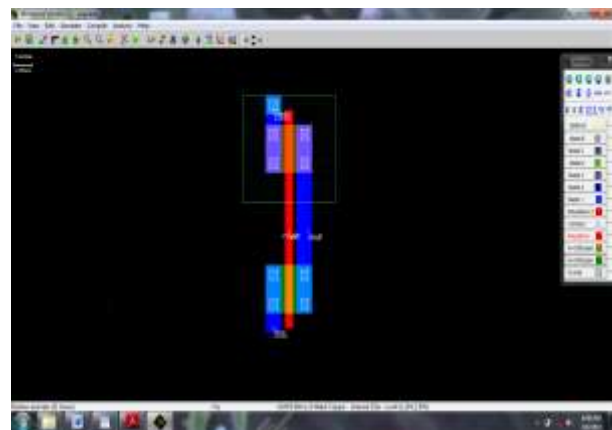


Fig. 20 Layout of inverter transistor

The inverter consists of an NMOS and a PMOS connected in series. The P_{SWITCH} is connected from a '1' source i.e. the VDD to the output and input The N_{SWITCH} is connected from a '0' source i.e. the GND to the output and the input.

1. Simulation of inverter

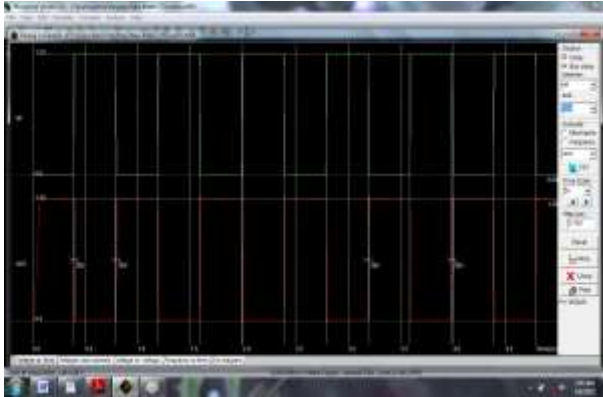


Fig. 21 Voltage Vs Time inverter transistor

In inverter when input is high it gives output low. And when input goes to low its output goes to high.



Fig. 22 Voltage Vs Current inverter transistor

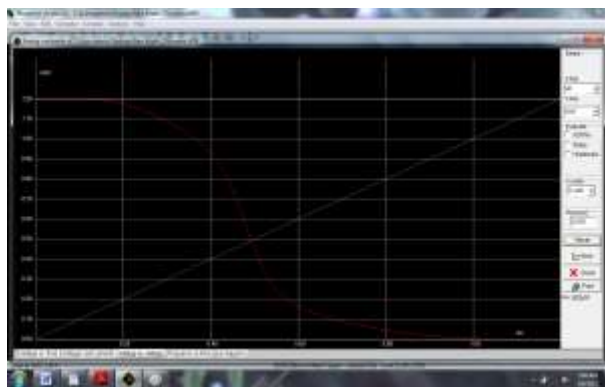


Fig 23 Voltage Vs Voltage inverter transistor

2. Layout design of 1-BIT SRAM(6T)

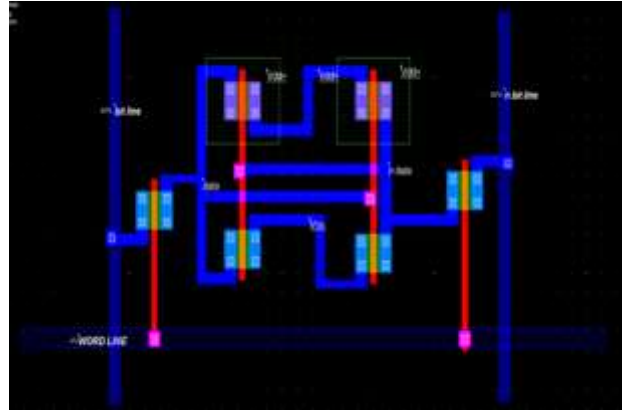


Fig. 24 Layout design of 1-BIT SRAM (6T) gate

Simulation of 1-BIT SRAM (6T)

Figure shows simulation of 1-bit SRAM. This is a voltage vs time waveform of

1-bit SRAM.

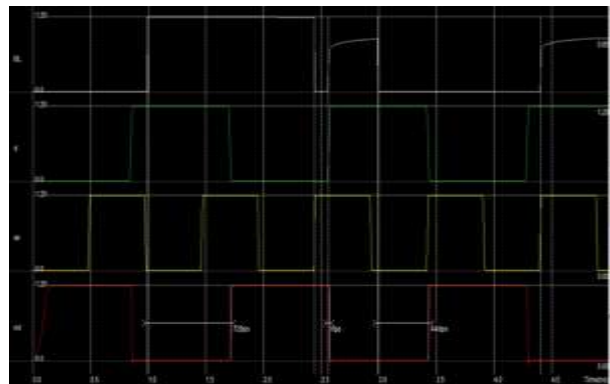


Fig. 25 voltage vs time SRAM gate

Figure shows simulation of 1-bit SRAM. This is a voltage and current waveform of

1-bit SRAM.

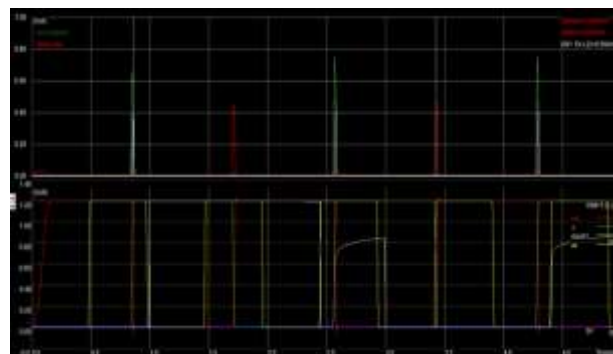


Fig. 26 Voltage and current wave form of SRAM gate

E. Layout design of 64-BIT SRAM by using 90nm Technology

Figure shows Layout design of 64-BIT SRAM by using 90nm Technology.

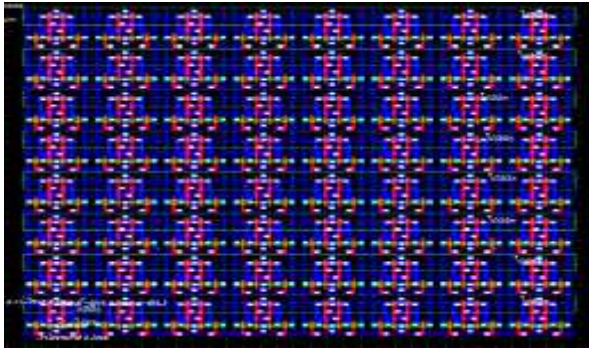


Fig. 27 Layout design of 64-BIT SRAM by using 90nm Technology

F. Simulation of 64-BIT SRAM by using 90nm Technology

Figure shows simulation of 64-bit SRAM by using 90nm Technology. This is a voltage and time waveform of 64-bit SRAM by using 90nm Technology.

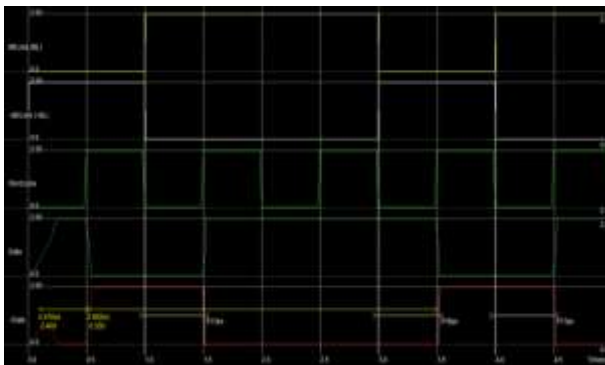


Fig. 28 Voltage Vs Time wave form of 64-BIT SRAM by using 90nm

G. Technology

At the point when the word line esteem is shown with high bit lines in the yield. In the event that the secret key line has low bit lines, unlink the word line and the square will keep the past esteem. The figure shows the recreation of a 64-bit SRAM utilizing 90 nm innovation. This is a voltage and current waveform of a 64-bit SRAM utilizing 90nm innovation.

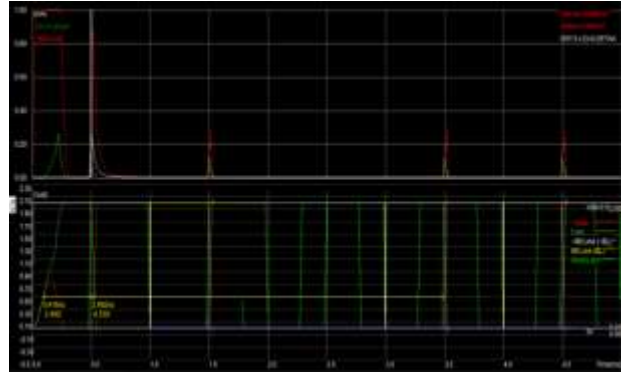


Fig. 29 Voltage and current waveform of 64-BIT SRAM by using 90nm Technology

H. Layout design of 1-BIT SRAM (5T) by using 90nm technology

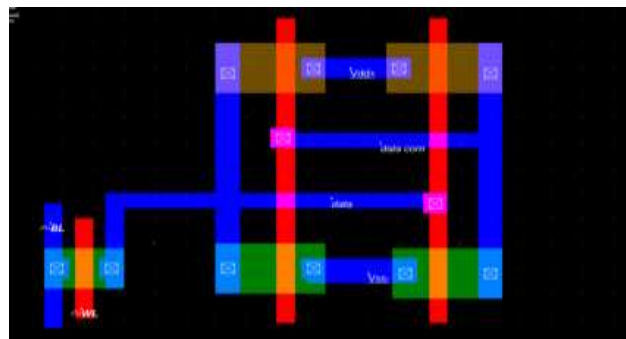


Fig. 30 Layout design of 1-BIT SRAM gate

The CMOS OR gate was designed by inverting the CMOS NOR gate. The OR output is high only when both or one of the inputs is high; H. The output will be weak only when both inputs are weak.

1. Simulation of 1-BIT SRAM (5T) by using 90nm technology

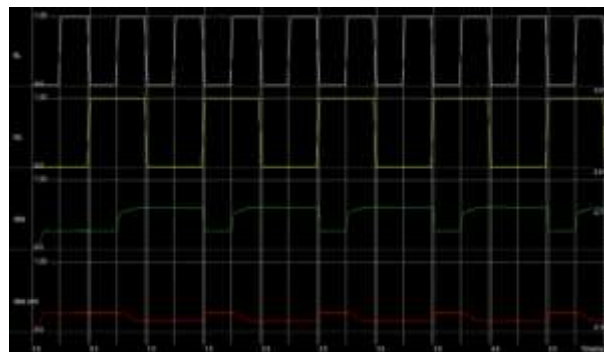


Fig. 31 voltage vs time SRAM gate

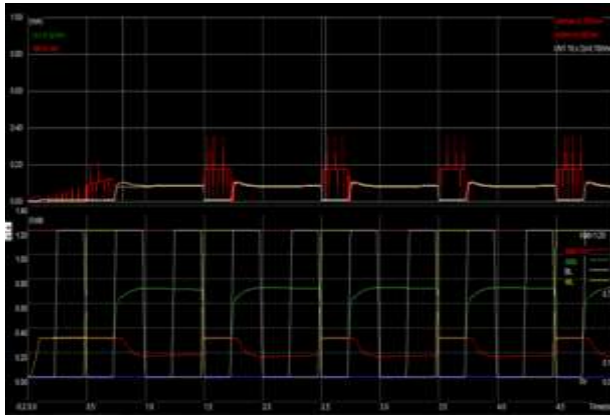


Fig. 32 Voltage and current wave form of SRAM gate

In a particular cell value on bit line goes in output when word line of cell is goes to high.



Fig. 35 Voltage and current waveform of 64-BIT SRAM

I. Layout design of 64-BIT SRAM gate(5T) by using 90nm technology

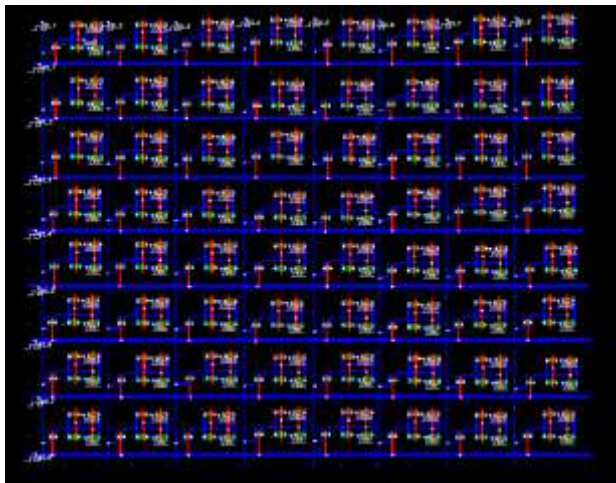


Fig. 33 Layout design of 64-BIT SRAM gate

Table 1 Comparison table of 5T and 6T SRAM

| Parameters | Bit 6T | Bit 5T |
|-------------------|---------------------|---------------------|
| Power dissipation | 2.184 μm | 1.076 μm |
| Leakage current | 0.150ma | 0.104ma |
| area | 4.83 μm | 4.68 μm |
| NO. of Transistor | 6 | 5 |

Table 2 Comparison table of 64 bits 5T and 64bit 6T SRAM

| Parameters | Bit 6T | Bit 5T |
|-------------------|----------------------|----------------------|
| Power dissipation | 37.479 μm | 5.402 μm |
| Leakage current | 0.257ma | 0.009ma |
| area | 301.76 μm | 289.12 μm |
| NO. of Transistor | 469 | 320 |

V. CONCLUSION & FUTURE SCOPE

This segment contains ends dependent on the consequences of practical reproduction and the execution of SRAM. Utilizing 0.12 micron and 90nm innovation, we plan 5T SRAM and we can peruse and compose. It is a principal part of a PC's focal preparing unit. Slam is a structure block comprising of a few circuits. The 64-bit SRAM drive was created with MICROWIND and DSCH2. With the MICROWIND program, the engineer can plan and recreate a coordinated circuit at the actual depiction level. DSCH2 permits exchanging of computerized rationale plan.

The actual plan (veil format) of the CMOS rationale entryways is an iterative cycle that starts with the geography of the circuit (to accomplish the ideal rationale work) and the underlying estimating of the semiconductors (to accomplish the ideal presentation particulars).

Future work might be reached out to advance SRAM with drive limit. Knowing which creation run is utilized and the pace of mistakes in the process gives us input on the plan with more modest capacitors. By executing rationale plans with more modest capacitors, power misfortune is diminished and the

1. Simulation of 64-BIT SRAM gate by using 90nm technology

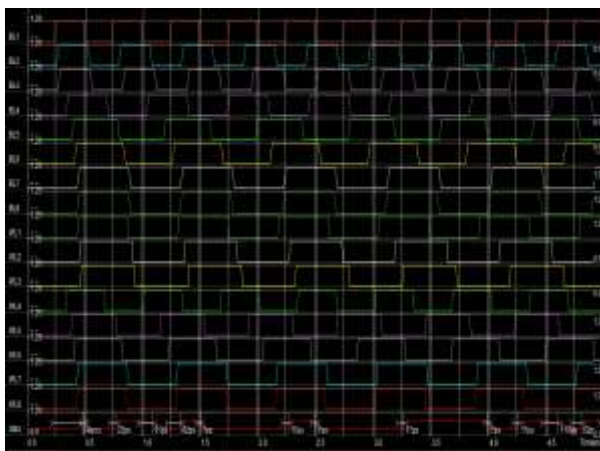


Fig. 34 Voltage vs Time wave form of 64-BIT SRAM

format is made more region proficient. Other work may likewise incorporate adding more info pieces to SRAM to the current task. Later on, two SRAMs will be utilized to execute fine-grained parallelism directions simultaneously.

REFERENCES

- [1] John R Hu, James Chen “Systematic co-optimization from chip design, process technology to systems for GPU AI chip”, 2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 16-19 April 2018.
- [2] M. Horowitz, “Computing’s energy problem (and what we can do about it),” in ISSCC Digest of Technical Papers, Feb. 2014, pp. 10–14.
- [3] M. Taylor, “Is dark silicon useful? Harnessing the four horsemen of the coming dark silicon apocalypse,” in Proc. of the Design Automation Conf., Jun. 2012, pp. 1131–1136.
- [4] T. Chen et al., “DianNao: A Small-footprint High-throughput Accelerator for Ubiquitous Machine-learning,” in Proc. of Intl. Conf. on Architectural Support for Programming Languages and Operating Systems, 2014, pp. 269–284.
- [5] Z. Wang, K. H. Lee, and N. Verma, “Hardware specialization in lowpower sensing applications to address energy and resilience,” Journal of Signal Processing Systems, vol. 78, no. 1, pp. 49–62, 2014.
- [6] H. Momose, Tatsuya Kaneko and Tetsuya Asai “Systems and circuits for AI chips and their trends” Japanese Journal of Applied Physics, Volume 59, Number 5, 2020.
- [7] Y. Chen, YuanXie “A Survey of Accelerator Architectures for Deep Neural Networks” Engineering Volume 6, Issue 3, March 2020, Pages 264-274.
- [8] Tso-Bing Juang,, Cong-Yi Lin and Guan-Zhong Lin “Area-Delay Product Efficient Design for Convolutional Neural Network Circuits Using Logarithmic Number Systems” ISOC 2018.
- [9] G. Grewal, S. Areibi, M. Westrik, Z. Abuowaimer and B. Zhao, "Automatic Flow Selection and Quality-of-Result Estimation for FPGA Placement," 2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), Lake Buena Vista, FL, 2017, pp. 115-123.
- [10] W. J. Chan, P. Ho, A. B. Kahng, P. Saxena, “Routability Optimization for Industrial Designs at Sub-14nm Process Nodes Using Machine Learning,” Proceedings of the 2017 ACM on International Symposium on Physical Design (ISPD 17), pp. 15-21.