DOI: https://doi.org/10.24113/ijoscience.v3i6.36

Less Power Consumption Based Low Delay Based 9-Transistors Based Full Adder

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***Abstract*— Circuit model of computer is widely accepted as a better abstraction of computational process across the world. The building block of a circuit is the logic gates which are the main information processing units. But this gates use higher power consumption. To reduce this power consumption researcher go on transistors. Transistors based design will gain increasing interest in industrial applications if they satisfy the following requirements: Less power requirement and reduced time with reduced design effort. The aim of this work is to contribute to reach these requirements for the design of full adders. In this paper, we present efficient full adder implementations using the transistors. The proposed design is based on a novel NMOS and PMOS transistors.**

Indexkey – Power consumption, Delay, SUM, Carry, Cin, Cout, Full Adder

I. INTRODUCTION

Full Adder is presumably the most essential component in all math module plan. Various full viper outlines have been proposed focusing on different plan accentuations, for example, power, speed and circuit many-sided quality. Among them, low transistor include full snake plans pass transistor rationale (PTL) have been effectively sought after to lessen the circuit multifaceted nature for low power operations. Outlines utilizing as few as 10 transistors (10-T) were accounted for in the writing [4-6]. Despite the circuit straightforwardness, these outlines experience the ill effects of extreme yield flag corruption issue and can't maintain low voltage operations [7]. In this paper, another 10-T full viper configuration went for easing these inadequacies is displayed. The key of the outline is the work of a worsen (sensibly inadequate) XOR-XNOR module utilizing just 5 transistors. In spite of the fact that the module is not consistently entire under all information blends, it is adequate to work legitimately in full viper applications. Its capacity of giving reciprocal "proliferate" control signals lessens the voltage corruption in the yield era stages. Contrasted with its outline partner [8], the proposed XOR-XNOR configuration is likewise free of DC power utilization and lock breaking issue. Consolidating the 5T XOR-XNOR rationale with multiplexer based "aggregate" and "convey" modules prompts our 10T full snake outline. Broad reenactments are directed to demonstrate the benefits of our outline.

With the blast of versatile PCs and other convenient gadgets, low-power and low-vitality configuration turned into an absolute necessity. Power and vitality go as an inseparable unit, control decrease prompts bring down vitality utilization over a settled time traverse. Math circuits are extensive benefactors of force and vitality in calculation concentrated applications and require along these lines a cautious power-defer plan tradeoff [1-3].

Expansion is an essential arithmetical operation in numerous VLSI frameworks, for example, DSP and microchip. Spread deferral, control utilization and power-postpone item (PDP) are the noteworthy quality measure parameters for a large portion of full snake frameworks, and the full viper would

influence the general execution of the framework. That is the reason streamlining the productivity of expansion is an always appealing exploration subject. The XOR-XNOR circuits are essential building obstructs in different full viper cell circuits [4].

In this paper, a complete approach for breaking down is exhibited. It depends on examined the snake cell into little modules, then utilize recreation to quantify the execution of each of them. Taking after this strategy we can locate the best reasonable module, then by amassing the modules together we frame a completely viper circuit which will be streamlined for low power.

So as to enhance the thorough execution, the creator may make a portion of the tradeoffs through the circuit configuration styles, design and calculation streamlined of the snake. There are ordinary executions with various circuit styles that have been utilized as a part of the past to configuration full-viper cells [5] and are utilized for examination in this paper. In spite of the fact that, they all have comparative capacity, the method for creating the interior hub capacitance and the topological structure is fluctuated. Distinctive rationale styles tend to support one execution viewpoint to the detriment of the others. The rationale style utilized as a part of rationale doors fundamentally impacts the engendering time, control scattering, and PDP[8-11].

Actualized, tried, and looked at. In Section 4, we exhibited distinctive full snake cells recreation results and analyze these viper cells in light of force utilization, speed, PDP in various test condition. At last, execution correlations and conclusions are exhibited [12].

II. LITERATURE REVIEW

A low power, low complexity full adder design based on degenerate pass transistor logic (PTL) is described. The design kernel is a logically degenerate 5-transistor XOR-XNOR module supporting complementary outputs. In spite of the logic deficiency, this module functions properly in the context of full adder applications. The threshold loss problem common in most PTL designs can be alleviated due to the availability of complementary control signals. Combining this module with multiplexing modules, a novel full adder design using as few as 10 transistors us derived. The proposed full adder design features the least output signal degradation and the smallest Vdd operations against other 10-T counterpart designs. The performance edges in speed, power and power-delay product are also proved via post layout simulations [24].

In present work two new designs for single bit full adders have been presented using three transistors XOR gates. Adder having twelve transistors shows power consumption of 1274μW with maximum output delay of 0.2049ns. Power consumption and maximum output delay shows variation [1274 - 141.77] μW & [0.2049 – 0.4167] ns with varying supply voltage from [3.3 - 1.8] V. Further, reverse body bias technique for power reduction has been applied to adder. Adder with reverse body bias shows power consumption variations of [1270 - 1067.60] μW with varying NMOS reverse bias from [0.0 to - 2.0] V. Delay of adder shows variations [0.2049 - 0.2316] ns with reverse bias variation [0.0 to 2.0] V. Simulations have been carried out at different supply voltage with increasing reverse biased applied to NMOS transistor and results shows improvements in power consumption of adder. A comparison with earlier reported circuits have been presented and proposed circuit's shows less power dissipation[25].

III. PROPOSED WORK

There are various ways to design the adder circuit. This article is all about the full adder design. This article design is based on transistors. Because of these PMOS and NMOS transistors the circuit become more efficient. This section shows the proposed design of the full adder, where PMOS passes 1 and NMOS passes 0.

Figure 5 shows the design of the proposed full adder based on transistors.

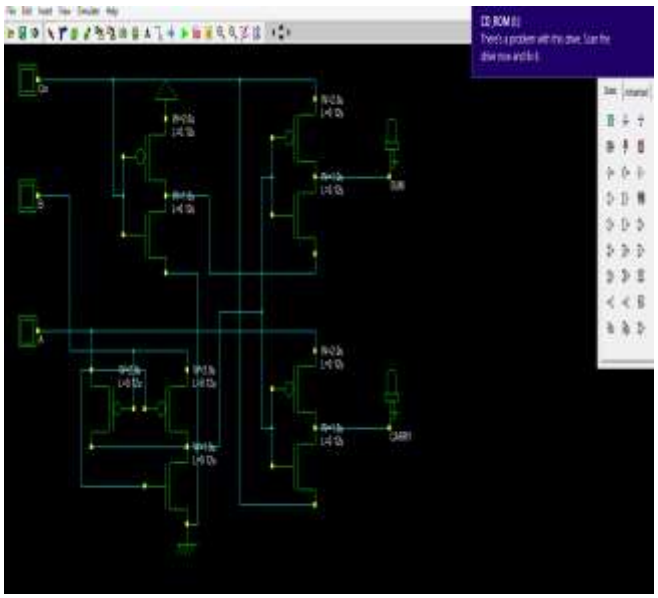


Figure 4: Proposed Design

IV. RESULT ANALYSIS

This section deals with the result of the proposed work along with the some previous results shown in figure 6.

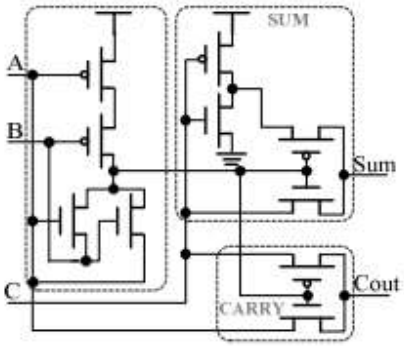


Figure 6[a] : 13A

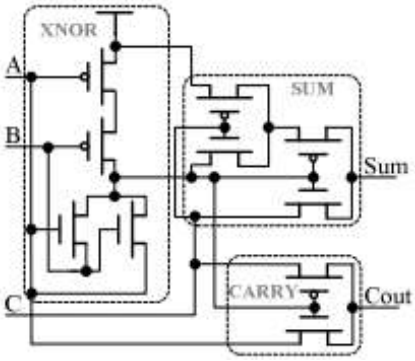


Figure 6[b] : 9A

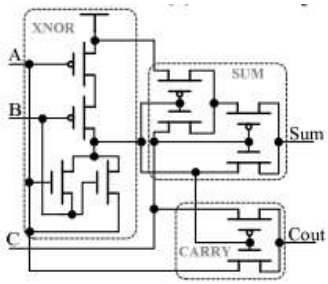


Figure 6[c]: 9B

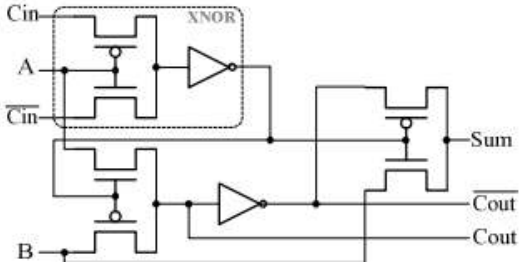


Figure 6[d]: CLR-CL

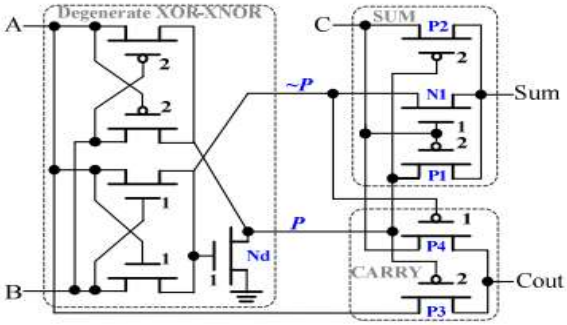
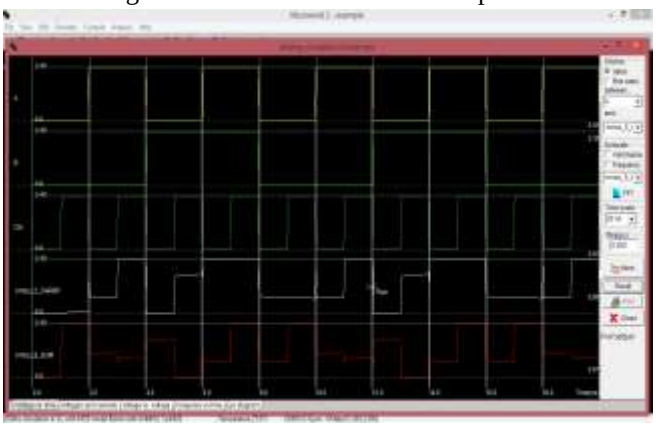


Figure 6[e] : Base Work[26]

This section is dedicated to represent the effectiveness of any design. This design is made up of 9 transistors and its structure. Figure 7 shows the various results parameters like



delay of sum, carry etc, power consumption, time slots,

Figure 7: It shows power consumption and Delay of proposed full adder

Following table I show the calculation of the power delay product.

Power-delay Product: It is a parametric quantity which measures the efficiency of the any circuit. This is a joint value and calculated as follows:

PDP (Power Delay Product) = Power Consumption* Delay of last product ….. (1)

Table II: Power delay Product

	13A [27]	9A [27]	9B [27]	CLRCL [28]	CP-FA [29]	Existing Work [26]	Our Work
Power Consumption (uW)	39.01	36.68	43.07	39.82	38.24	33.25	48.680
Carry Delay (nS)	3.84	4.11	3.92	1.52	2.18	0.85	0.011
Power-Delay-Product (pJ)	148.8	150.75	168.83	60.53	83.36	28.26	0.53548

From table II , it is clear that the proposed work is far better than existing work with the 9 transistors.

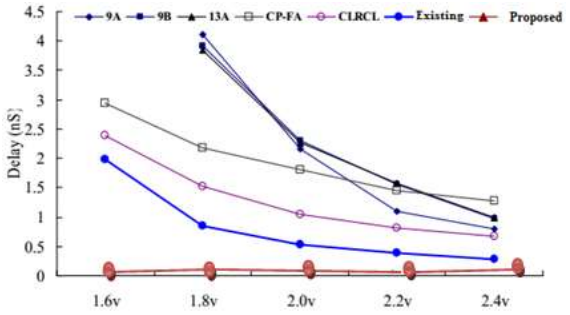
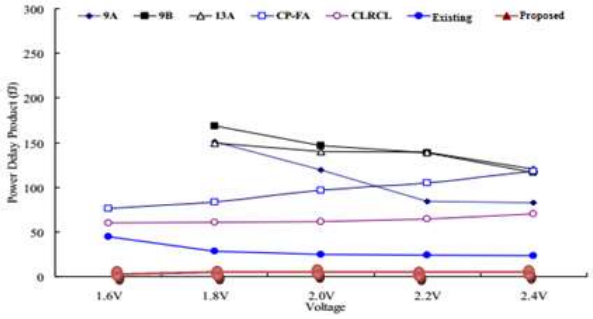


Figure 8: Proposed design performances versus supply voltages (a) Delay.



Supply Voltage

Figure 8: Proposed design performances versus supply voltages (a) Delay. (b) Power-Delay– Product

V. CONCLUSION

In this paper, we proposed new 9-transistor full adder. This adder is efficient on power consumption and the delay of the circuit. The proposed full adder had been designed and analyzed using Dsch and Microwind. In order to evaluate the usefulness of the proposed scheme, a proposed full adder was implemented, simulated and analyzed. This scheme combine two CMOS styles: pass transistor CMOS technology to perform the sum function and static CMOS technology for the carry gate. In addition, this scheme costs only 9 transistors, it requires the lowest hardware overhead. This simulation result clearly shows that the proposed design performs better than other transistors based adder in various metrics such as power, delay and power-delay product.

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