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Estimation of Delay to Consider Leakage in CMOS VLSI Circuit

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***Abstract*—In digital CMOS circuits, parametric yield improvement may be achieved by reducing the variability of performance and power consumption of individual cell instances. In recent years, increasing demand of portable digital systems has led to rapid and innovative development in the field of low power design. Such improvement of variation robustness can be attained by evaluating parameter variation impact at gate level. Statistical characterization of logic gates are usually obtained by computationally expensive electrical simulations. An efficient gate delay variability estimation method is proposed for variability-aware design. As the technology scaled down to deep nanometer level, the power supply, threshold (Vt) and device geometry gets reduces. The sub threshold current continue to increase exponentially, when the Vt of the device is reduced. The leakage current is now a dominant part of total power dissipation as the technology scales down. The proposed method has been applied to different topologies (transistor network arrangements) and CMOS gates, and it has been compared to Monte Carlo simulations for data validation, resulting in computation time savings.**

Keywords—Power optimization, Cmos Circuit, Leakage Current, Low Power

I. INTRODUCTION

CMOS circuit is initial part of chip. Chip is main component of digital revolution. o limit the power consumption, it is necessary to reduce the power consumption. This force the innovative developments in low power design. Leakage power dissipation is eventually becoming comparable to dynamic power dissipation in many high performance designs. The very large level of integration results in complication of heat removal ,this in turn increases the cost of cooling and packaging. Several researchers have proposed several methods to control the leakage power consumption. Kumar and Kursun (2006) presented a design methodology based on optimizing the supply voltage for temperature variation insensitive circuit. Self Controlled Stacked Transistor (SCST) or Leakage Control Transistor (LCT) technique (Hanchate and Ranganathan, 2004) is the technique to reduce leakage power consumption in CMOS gates without affecting the dynamic power of the circuit. In its 'off' state leakage control transistors acts as dynamic switch to reduce current flow, the operation of the switch is controlled by the current flowing in the branch of switch. Dual threshold transistors are used to reduce the leakage power consumption within given delay constraints. Leakage control transistors used in self-controlled stacked transistor technique are replaced by transistors having high threshold voltage (Verma and Mishra, 2012). Fig. 1(a) shows the LCT based two input NAND gate circuit having Mt1 and Mt2 as leakage control self bias stack transistors. Gate of p-channel and n-channel MOSFET is connected to the drain terminal of n-channel and p-channel MOSFET respectively. Voltage at drain terminal controls the operation the these leakage control transistors (LCTs) (Hanchate and Ranganathan, 2004).

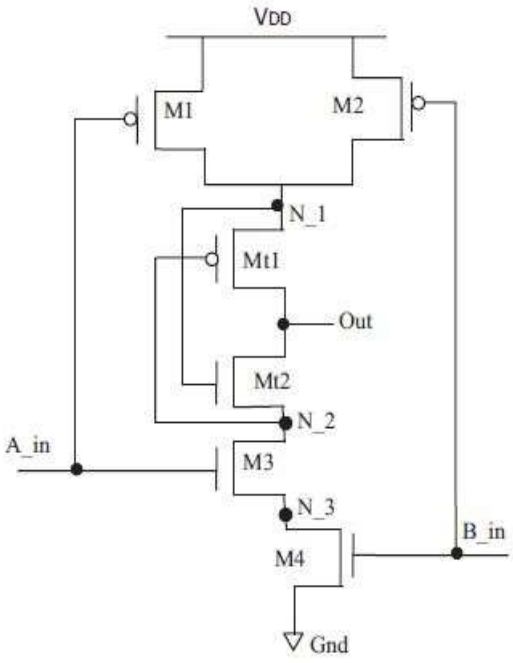

Figure 1 LCT NAND gate

Fig. 1(b) represents the application of high threshold transistor technique on NAND gate circuit. Here Mt1 and Mt2are the high threshold transistors, one of these two transistors always operates in its cutoff region. This results in an increase of number of OFF transistor from supply voltage to ground path and thus increasing stack effect. conclusion Leakage power consumption is measured by exciting the circuits with the same set of input vectors.180-nm process technology parameters are taken for the analysis of the circuits. Power is measured and average is done for all the input vectors to obtain the average leakage power dissipations. The advantage of both high threshold and stack effect is utilized to reduce power consumption. Delay of any path in the circuit depends on the delay of cells and nets. Path delay of digital circuit defines the performance of circuit.

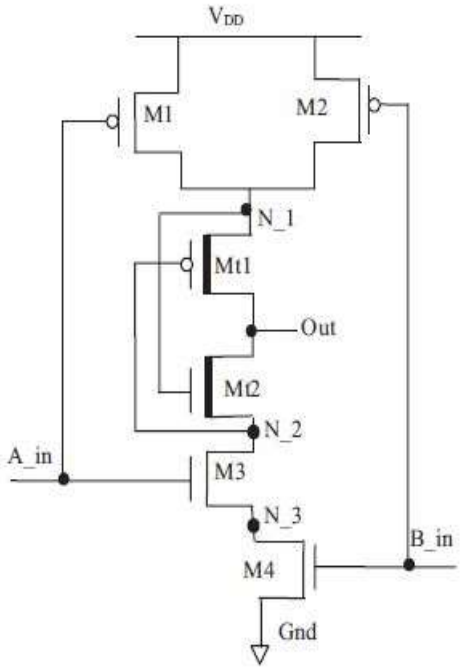

Figure 2 HTLCT based NAND gate.

II. RESULTS AND DISCUSSION

Experimental data, shown in the next sections, were obtained taking into account the 45 nm bulk CMOS PTM technology, using transistor channel

Table 1
Combinations of min and max values considered for the threshold voltages variations of devices in a 3-transistors network

Cases	Stack-03		
	V_{th1}	V_{th2}	V_{th3}
1	1	1	1
2	1	1	1
3	1	1	1
4	1	1	1
5	1	1	1
6	1	1	1
7	1	1	1
8	1	1	1

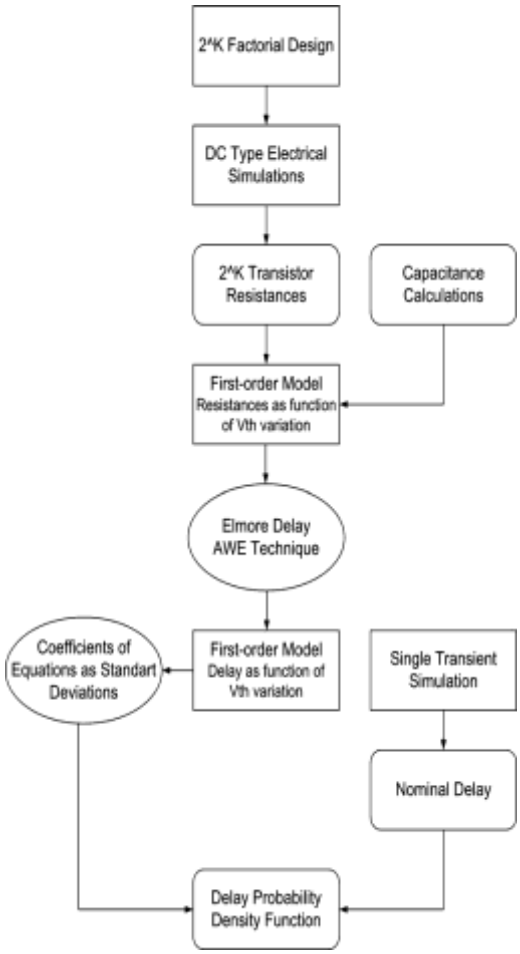

Figure 3 Gate delay variability estimation method flow

length (L) of 45 nm and width (W) varying from 90 nm to 180 nm. Electrical simulations were carried out through Taner.

(a) Series networks

Tables 2 and 3 present the normalized delay deviation for NMOS and PMOS transistor stacks, with three and four devices (stack-03 and stack-04, respectively), according to the

position of the switching transistor in relation to the output node, as illustrated in Fig. 4a.

The application of the AWE procedure presented better predicted delay deviations for the switching device far from the output node than for transitions in devices closed to the gate output. One can also observe a small reduction in delay variability when more stacked transistors are present, for both simulated and estimated results, but not for the case of 'close switching devices. According to the statistical simulations performed, close switching' causes higher delay deviation independently on the number of transistors in the stack.

Table 2
Delay deviation for NMOS transistors in series configuration, according to the position of the switching transistor in relation to the output node (1-close...4-far, as seen in Fig. 4a).

Switching transistor	Stack-03		
	Method w/Elmore	Method w/AWE	Monte Carlo
1	0.0472	0.0258	0.0434
2	0.0386	0.0277	0.0381
3	0.0272	0.0318	0.0361
4	-	-	-

Stack-04			
	Method w/Elmore	Method w/AWE	Monte Carlo
1	0.0448	0.0293	0.0423
2	0.0377	0.0246	0.0346
3	0.0268	0.0273	0.0311

Table 3
Delay deviation for PMOS transistors in series configuration, according to the position of the switching transistor in relation to the output node (1-close...4-far, as seen in Fig. 4a).

Switching transistor	Stack-03		
	Method w/Elmore	Method w/AWE	Monte Carlo
1	0.0218	0.0216	0.0379
2	0.0197	0.0198	0.0301
3	0.0188	0.0176	0.0281
4	–	–	–

Stack-04			
	Method w/Elmore	Method w/AWE	Monte Carlo
1	0.0188	0.0210	0.0403
2	0.0172	0.0155	0.0297
3	0.0163	0.0159	0.0261

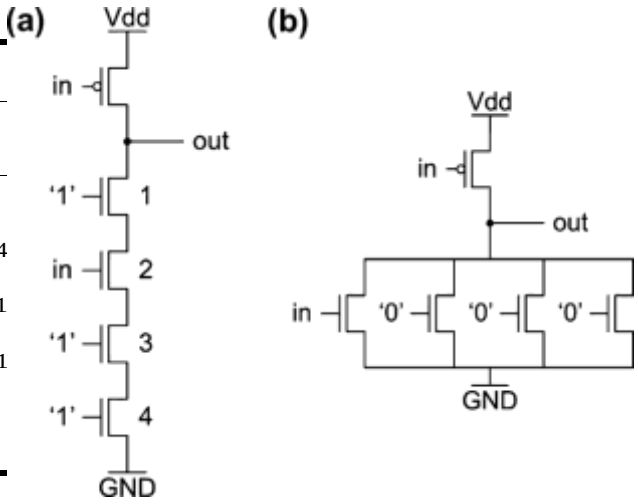

Figure 4. Test structures: (a) stacked and (b) parallel devices

(b) Parallel networks

Tables 4 and 5 present the normalized delay deviation for NMOS and PMOS transistors placed in parallel arrangement in the networks, as illustrated in Fig. 4b. The metrics are presented considering 1, 2 or 3 transistors switching at the same time, with the other(s) device(s) turned-off. The equivalent resistance of the parallel arrangement is applied to get the RC time constant. Statistical Monte Carlo simulations presented larger delay deviation for parallel NMOS networks than for the series arrangement. The results provided by the proposed method agreed

well with that. Transistors that are not conducting present small influence on the delay deviation of the structure and the delay model adopted (Elmore and AWE) presenting no significant influence on the procedure. According to the simulations, the increase of number of switching devices results in increasing delay deviation. However, the method does not handle the impact of multiple switching on delay deviation, since it presents lower delay deviation as the number of switching transistors increases. In the case of PMOS transistor networks, the proposed method agrees with the simulation results when it comes to how the number of switching devices impacts the delay deviation: the larger the number of switching transistors, the smaller the delay deviation. Also, both results point to no influence of the turned-off devices on this metric.

(c) CMOS inverter topologies

The delay variability estimation method has also been applied to different CMOS inverter topologies, illustrated in Fig. 5, and the results are presented in Table 6. The total area of the pull-down NMOS and pull-up PMOS networks was kept constant for all configurations presented. In order to investigate the influence of the area on the standard deviation of V_{th} and consequently on the delay of the logic gate, different variations were considered for different sizes by applying the relation between the parameter variation and the area provided by the Pelgrom's model.
The method presented delay variability values in agreement to the simulated results when it concerns to the topology less affected by DV_{th} for the rising- and falling-edge delays. In general, the method underestimated the delay variability for both NMOS and PMOS networks evaluated.

Table 4
Delay deviation for NMOS transistors in parallel association, according to the number of switching transistors.

Number of switching transistor	Parallel-03	
	Method[a]	Monte Carlo
1	0.0560	0.0519
2	0.0431	0.0536
3	0.0351	0.0619

Number of switching transistor	Parallel-04	
	Method[a]	Monte Carlo
1	0.0560	0.0505
2	0.0431	0.0503
3	0.0351	0.0578

[a] Only Elmore model were applied.

Table 5
Delay deviation for PMOS transistors in parallel association, according to the number of switching transistors

Number of switching transistor	Parallel-03	
	Method[a]	Monte Carlo
1	0.0361	0.0429
2	0.0257	0.0278
3	0.0209	0.0218

[a] Only Elmore model were applied.

Number of switching transistor	Parallel-04	
	Method[a]	Monte Carlo
1	0.0414	0.0430
2	0.0257	0.0276
3	0.0209	0.0213

0.0209

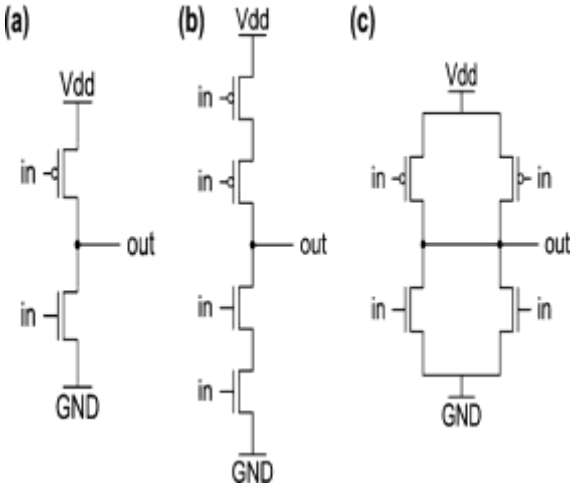

Figure 5. CMOS inverters: (a) conventional; (b) low leakage approach; (c) folded topology.

The characterization of the logic gates by using Monte Carlo approach is computationally very expensive. It takes a long time to be completed; for 10 k runs it may take more than hours, what makes it prohibitive as an estimator in a technology mapping context. The characterization based on transient simulations requires an execution time that is at least one order of magnitude higher than the proposed method. The approach presented in this work to characterize the cells is based on fast simulations, which take only few seconds, since only one of them is a transient simulation and all the others are DC type analysis. A significant speed-up was observed for the evaluated gates, which is important on a mapping context as many evaluations will be performed.

This work proposed a new method for predicting the delay variability of CMOS logic gates. It has been applied to different logic families, including not only the conventional static CMOS, but also differential structures like DCVSL and DPTL structures. The method provides reliable variability aware information at the cell level to choose among alternative implementations during technology mapping. The method is also efficient from an execution time stand point, which is important on a mapping context as many evaluations are performed during mapping.

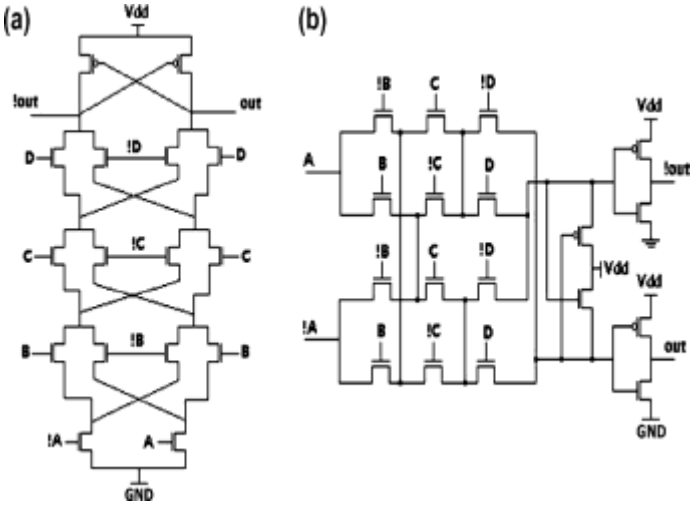

Fig. 5. Inverter Design using XOR4 (a) DCVSL and (b) DPTL

Table 8

Delay deviations for different implementations of a Inverter Design using 4-input XOR provided by the proposed method and the statistical Monte Carlo simulations

Logic style	Rise delay deviation	
	Method	Monte Carlo
DCVSL	0.0361	0.0426
DPTL	0.0351	0.0341

Fall delay deviation	Rise delay deviation	
	Method	Monte Carlo
DCVSL	0.0282	0.0261
DPTL	0.0717	0.1464

III. CONCLUSIONS

This work proposed a new method for predicting the delay variability of CMOS logic gates. It has been applied to different logic families, including not only the conventional static CMOS, but also differential structures like DCVSL and DPTL structures. The method provides reliable variability aware information at the cell level to choose among alternative implementations during technology mapping. The method is also efficient from an execution time stand point, which is important on a mapping context as many evaluations are performed during mapping. This way, the method fulfills the goal of providing reliable variability aware information at the cell level to choose among alternative implementations during technology mapping.

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